IN THE CLAIMS

Please amend the claims as follows:

18. (Amended) A trench capacitor comprising:

a crystalline silicon substrate including deep trenches having surfaces in the substrate substantially free of native oxide; and

C1

a dielectric stack, including a continuous monocrystalline silicon nitride layer, formed on the surfaces of the trenches, the dielectric stack for forming a node dielectric between electrodes of the trench capacitor.

23. (Amended) A trench capacitor comprising:

a crystalline silicon substrate including a trench having a surface formed in the substrate, the surface being substantially free of native oxide;

C2

a continuous monocrystalline silicon nitride layer, formed on the surface of the trench; and

an amorphous silicon nitride layer formed on the crystalline silicon nitride layer, the crystalline silicon nitride layer and the amorphous silicon nitride layer for forming a dielectric between electrodes.

REMARKS

This application has been reviewed in light of the Office action dated May 9, 2001. Claims 18-29 are now pending in the application. Claims 18 and 23 have been amended. No new matter has been added. The Examiner's reconsideration of the rejection in view of the following remarks is respectfully requested.

By the office action, claims 18-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over EPO 684,637 to Kasai et al. (Kasai) in view of U.S. Patent No. 5,643,823 to Ho et al. (Ho).

Kasai is directed to the formation of a low-pressure thermally deposited film. The film is deposited by a thermal process, which forms an amorphous film. A crystalline film or continuous crystalline film is not disclosed or suggested by Kasai, as suggested by the Examiner. Ho suggests a nitride layer, which forms crystallites, but is largely amorphous (see e.g., col. 3, lines 6-11 in Ho). In addition, the nitride layer is formed on a silicon oxide layer (see col. 2, lines 53-56 in Ho).

The present invention includes, *inter alia*, a trench capacitor with a crystalline silicon substrate including deep trenches having surfaces in the substrate substantially free of native oxide and a dielectric stack, including a continuous monocrystalline silicon nitride layer, formed on the surfaces of the trenches, the dielectric stack for forming a node dielectric between electrodes of the trench capacitor. The present invention provides a continuous monocrystalline layer. Support for the amendment is found throughout the specification. The cited references provide only an amorphous layer with crystallites (i.e., floating crystals) or just an amorphous nitride layer.

Further, the continuous monocrystalline layer of the present invention is formed on the surface of the substrate (see claims 18 and 23, for example). Kasai and/or Ho fail to disclose or suggest or suggest this. Instead, the cited references form the thermal nitride on an oxide layer. Therefore, the cited art fails to disclose the present invention as clarified by the amendments. Reconsideration of the rejection is earnestly solicited.

It is respectfully requested that the Examiner consider replacing the current rejections with an obvious-type double patenting rejection. In that case, the Applicants would consider filing a terminal disclaimer, if appropriate.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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